

A Modified Asymmetrical Pulse-Width-Modulated Resonant DC/DC Converter Topology

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Abstract—A modified asymmetrical pulse-width-modulated resonant dc/dc converter employing an auxiliary circuit will be proposed in this paper. The auxiliary circuit consists of a network of two capacitors and an inductor. The aim of this network is to produce zero-voltage-switching (ZVS) over a wide input voltage range, while reducing the voltage stress on the resonant component. A detailed analysis and performance characteristics are presented. Experimental results for a 5 V, 35 W converter show an efficiency of 83% at a constant operating frequency of 500 kHz. Using metal oxide semiconductor field effect transistors (MOSFETs) as synchronous rectifiers can further reduce power losses and improve the efficiency to be greater than 90%.

Index Terms—Auxiliary circuit, capacitor, dc/dc converter, inductor, MOSFET, pulse-width-modulated.

NOMENCLATURE

V_{in}	Input dc voltage.
D	Effective duty cycle for S_1 .
Q_o	Quality factor of the resonant tank.
ω_o	Switching frequency in rad/s.
f_o	Switching frequency in Hz.
f_r	Resonant frequency in Hz.
ω	Ratio between switching and resonant frequency.
R_{ac}	Equivalent output resistance as seen by resonant tank.
$N_P/N_S, n_{T_s}$	Transformer turns ratio.
$I_{r\ max}$	Peak of the fundamental resonant current.
V_{S2}	Drain-source voltage of S_2 .
θ_n	Phase angle due to asymmetrical duty cycle.
i_r	Resonant current.
ϕ_n	Phase angle due to resonant tank.
Z_{in}	Input impedance of resonant tank.
$v_{S2\ ac}$	AC component of v_{ds2} .
v_{La}	Voltage across auxiliary inductor.
i_{La}	Auxiliary inductor current.
δ_n	Phase angle of i_{La} .
$I_{La\ pk}$	Peak of the auxiliary current.
i_{sw}	Total current through S_1 and S_2 .
M	Voltage conversion ratio.
K	Ratio between auxiliary and resonant inductors.
I_2	Current at the turn-off of S_2 .

I_1	Current at the turn-off of S_1 .
v_{L_S}	Voltage across resonant inductor.

I. INTRODUCTION

IN ORDER TO meet the requirements of point-of-use power supplies in telecommunication and computer systems, many constant frequency resonant converter topologies have been reported in the literature [1]–[5].

The goal of these topologies is to try and achieve high power density, high efficiency, low switching losses while operating at a constant frequency. In examining these topologies, their switching losses are low and they can be operated at high frequencies. Also, they offer high power density at medium to high power levels. However, their component count is high resulting in lower power densities at low to medium power levels.

The asymmetrical pulse-width-modulated (APWM) resonant dc/dc converter topology [6], [7] has been presented and it offers near-zero switching losses while operating at constant and very high frequencies. Its component count is low, making operation at low to medium power levels feasible. The input voltage range over which ZVS is achieved is narrow, and the efficiency of the converter decreases as the input voltage is increased. Also, the resonant inductor incurs higher losses as the operating frequency is increased. This paper presents a modified APWM resonant dc/dc topology ([8, Fig. 1]) that can overcome the drawbacks described above.

Section II will give the description and operating principle of this modified topology. Section III will present the mode of operation during each of the four intervals of one cycle and key waveforms of the circuit. Section IV covers the steady-state analysis. Section V presents the performance curves that aid in the design of the network. Section VI gives the experimental results of a 35 W, 500 kHz prototype and Section VII provides a comparison of the original topology and the improved one.

II. MODIFIED APWM RESONANT DC/DC CONVERTER TOPOLOGY

Fig. 1 shows an APWM resonant dc/dc converter topology employing the additional network. This circuit can be broken into functional blocks: the auxiliary circuit (C_{1a}, C_{2a}, L_a), a chopper (S_1, S_2), a series resonant tank (L_s, C_s), a power transformer (T_x), Synchronous rectifier (SR_1, SR_2) and the output filter. The auxiliary circuit has the following functions:

- i) inductor L_a provides compensating current to achieve ZVS at higher input voltage;
- ii) capacitors C_{1a} and C_{2a} split the dc input voltage.

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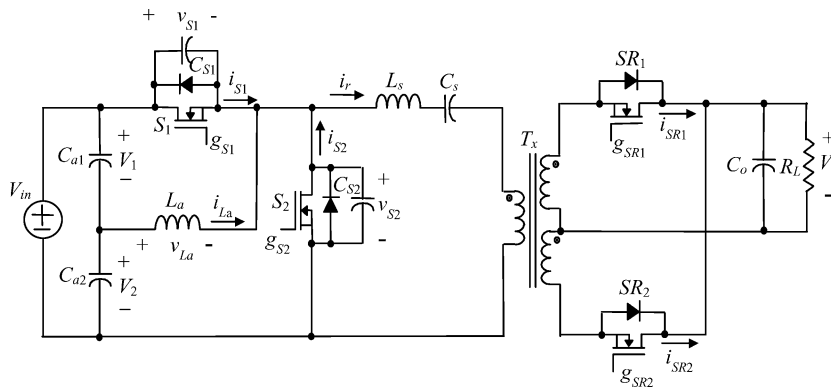


Fig. 1. Modified APWM series resonant dc/dc converter topology.

III. OPERATING PRINCIPLE

This circuit consists of two switches, S_1 and S_2 which are controlled by two compensating gating signals, g_{S1} and g_{S2} , respectively. The gating signal of S_1 has a duty cycle of D and that of S_2 is $1 - D$. When S_1 is on, the power from the source is transferred to the load and the output of the chopper sees a positive voltage of V_{in} from the source. When S_2 turns on, the source is separated from the rest of the power circuit and the output of the chopper sees the voltage across S_2 which is zero volts. The energy from the resonant components now freewheels through S_2 and supplies power to the load. By varying D we can control the output voltage. This requires a feedback network, which increases D if the output voltage becomes too low and vice versa.

The operation of this circuit can be seen in four intervals. Fig. 2 shows the key waveforms during each of these intervals. For each interval, the operation of the converter is described as follows.

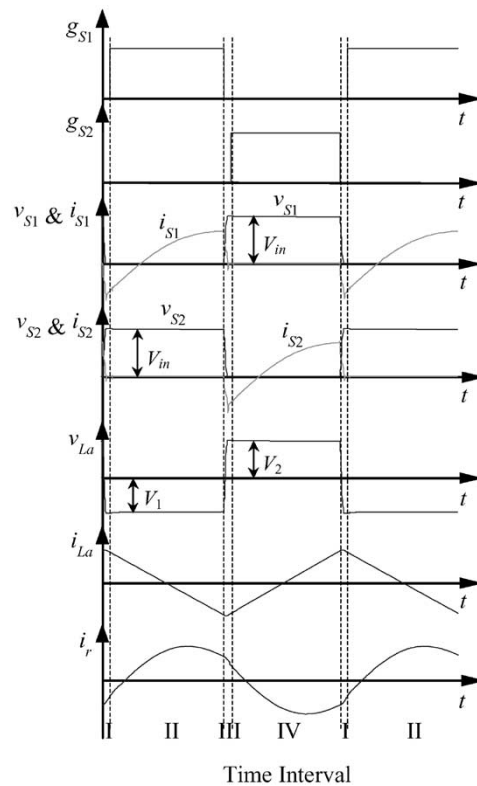


Fig. 2. Key operating waveforms of the circuit diagram in Fig. 1.

Interval I: Prior to this interval S_2 was on, and at the beginning of this interval, S_2 is switched off. The negative current flowing through the resonant branch and the positive current through the auxiliary inductor force the charging of C_2 and the discharging of C_1 . Once C_1 has fully discharged and C_2 has fully charged, the current forces the conduction of diode D_1 . The voltage across S_1 is now set at 0 volts, and the voltage across S_2 equals V_{in} . Meanwhile, the voltage across L_a changes from $(+V_2)$ to $(-V_1)$. V_1 and V_2 are the voltages across C_{a1} and C_{a2} , respectively, whose values are dependent on the duty cycle D and are given in Section IV. The current through L_a during this interval reaches its peak value and starts to decrease.

Interval II: At the beginning of this interval, gating signal g_{S1} is applied to the gate of S_1 to switch it on. The current previously flowing through D_1 now flows through S_1 . The switch thus turns on under zero voltage, and the output voltage of the chopper equals V_{in} . Power flows from the input dc source to the resonant circuit and to the output load. The voltage across L_a during this interval remains constant at $(-V_1)$, and the current through L_a keeps decreasing linearly.

Interval III: At the beginning of this interval, switch S_1 is turned off. The positive current flowing through the resonant branch and the negative current through the auxiliary

inductor force the discharging of C_2 and the charging of C_1 . Once C_2 has fully discharged and C_1 has fully charged, the current forces the conduction of diode D_2 . The voltage across S_2 is now set at 0 volts, and the voltage across S_1 equals V_{in} . Meanwhile, the voltage across L_a changes from $(-V_1)$ to $(+V_2)$, and the current through L_a reaches its negative peak value and starts to increase.

Interval IV: At the beginning of this interval, gating signal g_{S2} is applied to the gate of S_2 to switch it on. The current previously flowing through D_2 now flows through S_2 . The switch thus turns on under zero voltage, and the output voltage of the chopper is clamped to zero. The energy stored in the resonant components now flows through S_2 to supply power to the output load. The voltage across L_a during this interval remains constant at $(+V_2)$, and the current through L_a keeps increasing linearly.

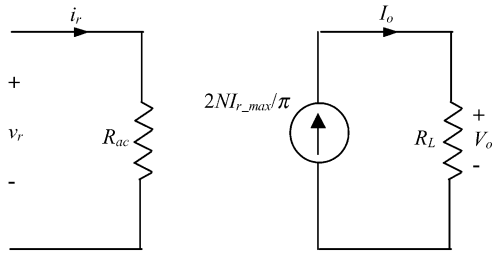


Fig. 3. Equivalent model of the ideal output stage.

IV. STEADY-STATE ANALYSIS OF THE CONVERTER

This section will present the steady-state analysis of the circuit in Fig. 1. In doing the analysis, the following assumptions are made.

- 1) The semiconductor switches and diodes are ideal.
- 2) The effect of capacitors across the switches is negligible.
- 3) An ac equivalent resistance at the primary of transformer represents the output rectification stage.
- 4) The delay time between the two switches is neglected.
- 5) The diode rectifier incurs zero losses.

The minimum input voltage, $V_{in,min}$ (volts), the equivalent ac resistance R_{ac} (Ω), and the resonant frequency ω_r (r/s) of the series resonant components are chosen as the base values. The following equations have been developed from the original circuit [7], but are still valid for this topology

$$Q_o = \frac{\omega_r L_s}{R_{ac}} \quad (1)$$

$$\omega = \frac{\omega_o}{\omega_r} \quad (2)$$

$$R_{ac} = \frac{8}{\pi^2} N^2 \cdot R_L \quad (3)$$

$$f_r = \frac{1}{2\pi \sqrt{L_s C_s}} \quad (4)$$

where ω_o is the operating frequency, R_L is the load resistance, N is the turns ratio of the transformer, and L_s and C_s are resonant inductance and capacitance, respectively.

In order to simplify the analysis, the circuit can be broken down into its functional blocks. Equation (3) shows how the output load is seen as an ac equivalent resistance by the resonant tank. An equivalent model of the output stage is shown in Fig. 3.

The next stage is the resonant tank network. The voltage at the input of the resonant tank is equal to the voltage, v_{s2} , across the switch S_2 . This can be represented in terms of Fourier series in one switching cycle, T_s as [7]

$$v_{s2}(t) = V_{in} D + \sum_n \left[\frac{\sqrt{2} V_{in}}{n\pi} \cdot \sqrt{1 - \cos 2n\pi D} \cdot \sin(n\omega_o t + \theta_n) \right] \quad (5)$$

where

$$\theta_n = \tan^{-1} \left[\frac{\sin 2n\pi D}{1 - \cos 2n\pi D} \right]. \quad (6)$$

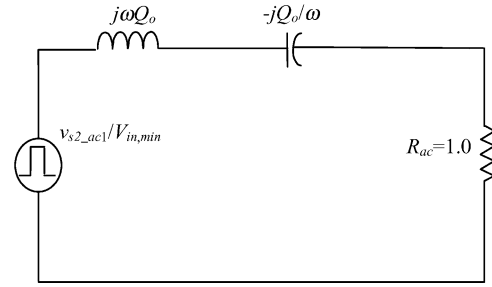


Fig. 4. Per unit equivalent fundamental model of the series resonant tank.

The per unit resonant current is derived from the ac component of v_{s2} , v_{s2_ac}

$$i_r(t) = \sum_n \frac{\sqrt{2} V_{in}}{n\pi |Z_{in}| V_{in,min}} \cdot \sqrt{1 - \cos 2n\pi D} \cdot \sin(n\omega_o t + \theta_n - \phi_n) \quad (7)$$

where

$$|Z_{in}| = \sqrt{1 + Q_o^2 \left(n\omega - \frac{1}{n\omega} \right)^2} \quad (8)$$

$$\phi_n = \tan^{-1} \left[Q_o \left(n\omega - \frac{1}{n\omega} \right) \right]. \quad (9)$$

From (7), the peak value of the fundamental resonant current, I_{r_max} can be given as

$$I_{r_max} = \frac{\sqrt{2} V_{in} \cdot \sqrt{1 - \cos(2\pi D)}}{\pi \cdot V_{in,min} \cdot \sqrt{1 + Q_o^2 \left(\omega - \frac{1}{\omega} \right)^2}} \quad (10)$$

The equivalent model of the fundamental of the resonant tank network is shown in Fig. 4.

The next stage to be considered is the switch and the compensating network. The switch currents are functions of both the resonant and auxiliary currents. The auxiliary inductor generates the auxiliary current. To solve for this current, the waveforms of the voltage across and current through the auxiliary inductor are redrawn in Fig. 5. Assume for simplicity that the dead time between gating signals g_{S1} and g_{S2} is zero in the following derivation.

Firstly, the voltages across the auxiliary capacitors C_{a1} and C_{a2} , V_1 and V_2 , respectively, have to be derived. Since C_{a1} and C_{a2} split the dc input voltage ($V_1 + V_2 = V_{in}$), and in Fig. 5, the time integral of the inductor voltage over one switching period must be zero ($V_1 D T_s = (1 - D) T_s V_2$) in the steady state, V_1 and V_2 can be obtained as

$$V_1 = (1 - D) V_{in} \quad (11)$$

$$V_2 = D V_{in}. \quad (12)$$

To derive the expressions of v_{La} and i_{La} , a new axis system (y', t') is built in Fig. 5 so that the function of v_{La} is an even function and can be expressed by the Fourier series as

$$v_{La} = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_o t') \quad (13)$$

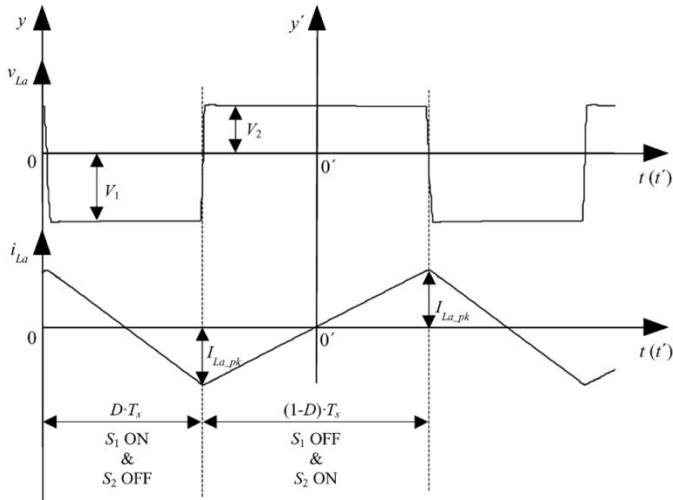


Fig. 5. Voltage and current waveforms of the auxiliary inductor.

where $a_0 = 0$, and

$$a_n = \frac{2V_{in}}{n\pi} \sin[n\pi(1-D)] \quad n = 1, 2, 3, \dots \quad (14)$$

Thus, i_{La} can be obtained as

$$i_{La} = \frac{2V_{in}}{\pi L_a} \sum_{n=1}^{\infty} \frac{1}{n} \sin[n\pi(1-D)] \left(\frac{1}{n\omega_o} \sin(n\omega_o t') + C \right). \quad (15)$$

Considering the initial condition $i_{La}(t' = 0) = 0$, the constant C is equal to zero. The peak value of i_{La} occurs at $t' = (1-D)T_s/2$ and equals

$$I_{La.pk} = \frac{1}{L_a} \int_0^{(1-D)T_s/2} V_2 dt = \frac{D(1-D)V_{in}}{2f_o L_a}. \quad (16)$$

Replacing t' by $t' = t - T_s(1+D)/2$ in (13) and (15), the expressions of v_{La} and i_{La} in the original axis system (y, t) are found as

$$v_{La} = \frac{2V_{in}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin[n\pi(1-D)] \times \cos[n\omega_o t - n\pi(1+D)] \quad (17)$$

$$i_{La} = \frac{2V_{in}}{\pi\omega_o L_a} \sum_{n=1}^{\infty} \frac{1}{n^2} \sin[n\pi(1-D)] \times \sin[n\omega_o t - n\pi(1+D)]. \quad (18)$$

Introducing a variable K which relates L_s to L_a as $K = L_a/L_s$, current i_{La} and its peak value can be normalized to their per unit expressions as

$$i_{La-pu} = \frac{2V_{in}}{\pi\omega_o Q_o K V_{in,min}} \sum_{n=1}^{\infty} \frac{1}{n^2} \sin[n\pi(1-D)] \times \sin[n\omega_o t - n\pi(1+D)] \quad (19)$$

$$I_{La.pk-pu} = \frac{\pi D(1-D)}{K\omega \cdot Q_o} \frac{V_{in}}{V_{in,min}}. \quad (20)$$

The per unit current through the switch is then the subtraction of the auxiliary current given by (19) from the resonant current

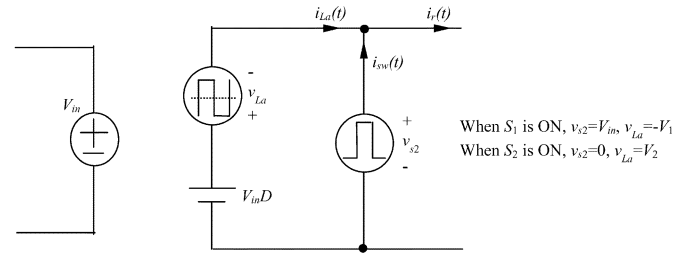


Fig. 6. Equivalent model of the switch network including the compensating network.

given by (7) during its conduction time. Fig. 6 illustrates an equivalent circuit for the switch network.

Now that each stage has been analyzed, the whole converter can be seen in its entirety. The voltage conversion ratio, M , is the ratio between the output and the input voltages. It is given by

$$M = \frac{V_o}{V_{in}} = \frac{2\sqrt{2}N \cdot R_o}{\pi^2} \cdot \frac{\sqrt{1 - \cos(2\pi D)}}{\sqrt{1 + Q_o^2 \left(\omega - \frac{1}{\omega}\right)^2}}. \quad (21)$$

V. PERFORMANCE CURVES OF THE CONVERTER

This section presents the performance characteristics of the converter. The analysis that was developed in the last two sections will be used in deriving the performance equations and curves. In the following derivation, with the selection of $K = 1$, the auxiliary inductor and the resonant inductor can have the same value, thus lowering production costs.

Turn-off current I_2 of Switch S_2 : In order to achieve ZVS for S_1 , the current at the turn-off of S_2 , as given by (22), must be negative. Fig. 7 shows I_2 as a function of D with the various values for Q_o and ω with $K = 1$

$$I_2 = \frac{V_{in}}{V_{in,min}} \left[\sum_n \frac{\sqrt{2}}{n\pi |Z_{in}|} \sqrt{1 - \cos 2n\pi D} \times \sin(\theta_n - \phi_n) - \frac{\pi D(1-D)}{K\omega \cdot Q_o} \right]. \quad (22)$$

Turn-off current I_1 of Switch S_1 : In order to achieve ZVS for S_2 , the current at the turn-off of S_1 given by (23) must be positive. Fig. 8 shows I_1 as a function of D with the various values for Q_o and ω with $K = 1$

$$I_1 = \frac{V_{in}}{V_{in,min}} \left[\sum_n \frac{\sqrt{2}}{n\pi |Z_{in}|} \sqrt{1 - \cos 2n\pi D} \times \sin(2n\pi D + \theta_n - \phi_n) + \frac{\pi D(1-D)}{K\omega \cdot Q_o} \right]. \quad (23)$$

Figs. 7 and 8 show that with the selection of Q_o between 1.5 to 2.5, and ω between 1.1 to 1.3, ZVS is achieved in the complete range of duty cycle control. Thus with the aid of the auxiliary circuit, the modified topology has ZVS over wider input voltage range compared with the original topology [7].

However, it is evident from the previous graphs that the values of Q_o and ω chosen affect the amount of current passing through the switches, and furthermore, increase the conduction losses of

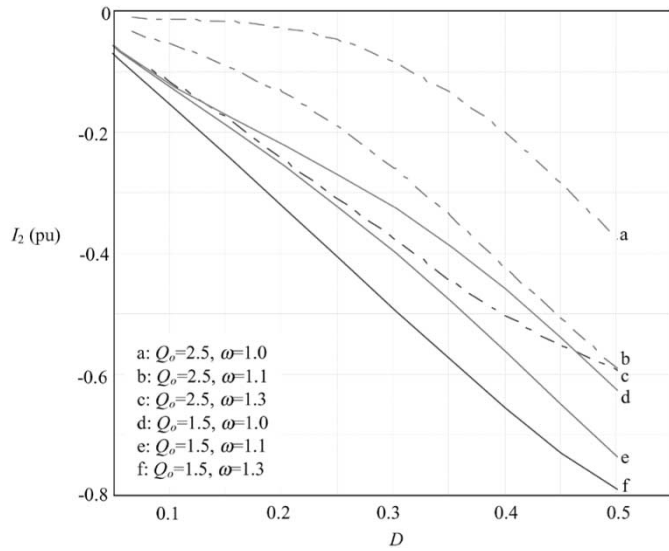


Fig. 7. Current through S_2 at turn-off, I_2 , as a function of D for $K = 1$.

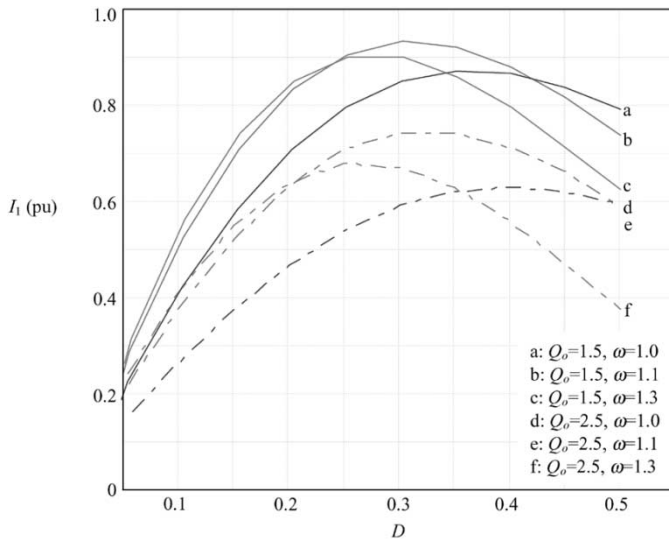


Fig. 8. Current through S_1 at turn-off, I_1 , as a function of D for $K = 1$.

the switches. To determine these losses, per unit fundamental switching current in Fig. 6 is calculated by (24). Harmonics are ignored because they have less contribution to the losses and produce prolix calculation

$$i_{sw1}(t) = \frac{\sqrt{2}V_{in}}{\pi V_{in,\min}} \left[\frac{\sqrt{1 - \cos 2\pi D}}{|Z_{in}|} \cdot \sin(\omega_o t + \theta_1 - \phi_1) + \frac{\sqrt{2}}{\omega K Q_o} \sin(\pi D) \sin(\omega_o t - \pi D) \right] \quad (24)$$

where $|Z_{in}|$, θ_1 , and ϕ_1 are given by (6), (8), and (9), respectively, when $n = 1$.

The RMS value of i_{sw1} is given by (25) and plotted in Fig. 9 as a function of duty cycle for various values of Q_o and ω with $K = 1$

$$i_{sw1}(t) = \frac{V_{in}}{\pi V_{in,\min}} \sqrt{\frac{1 - \cos 2\pi D}{|Z_{in}|^2} + \frac{2 \sin^2(\pi D)}{(\omega K Q_o)^2}} \quad (25)$$

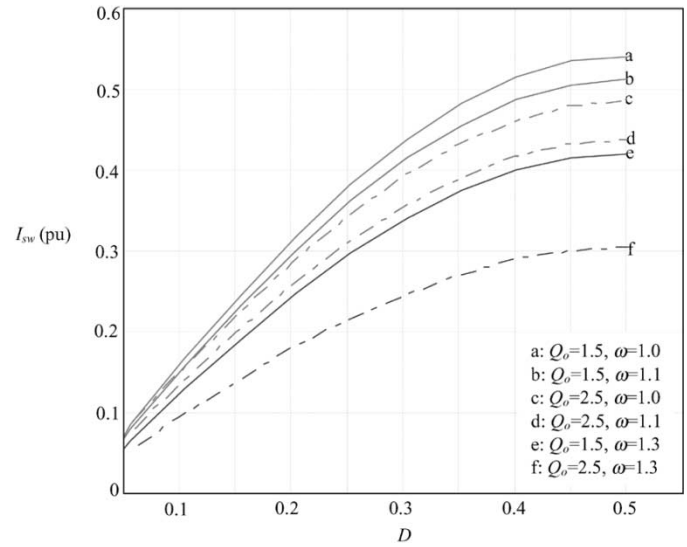


Fig. 9. Per unit RMS value of the fundamental switching current.

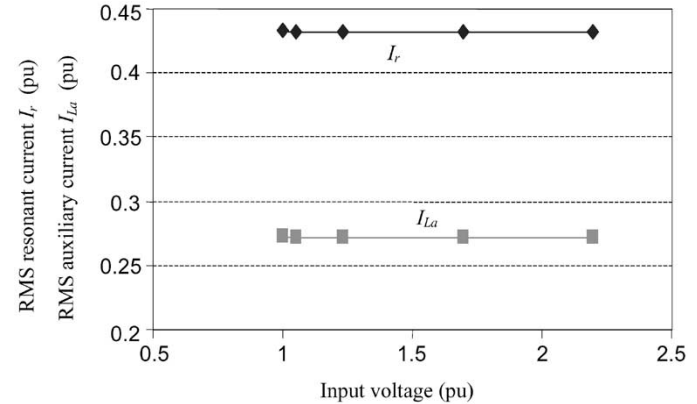


Fig. 10. Per unit RMS value of the fundamental resonant current and auxiliary current with variation of input voltage ($P_o = 1$ pu, $Q_o = 1.5$ and $\omega = 1.1$).

Fig. 9 shows that higher values of ω and Q_o result in lower current circulation in the switch. However, in general, higher values of ω and Q_o result in more power losses in the resonant tank (maximum power transfer without auxiliary circuit occurs at $\omega = 1$), and more voltage stress on the resonant component, which is proportional to Q_o . Therefore, some trade-off must be made during the specific design. It is found that the selection of $Q_o = 1.5$ and $\omega = 1.1$ is good for the input voltage range of 2:1.

For constant output power $P_o = 1$ pu, $Q_o = 1.5$ and $\omega = 1.1$, the RMS value of the fundamental resonant current and auxiliary current are shown in Fig. 10 for a varying input voltage range of 2:1. This figure shows that the auxiliary current will cause increased RMS current through the switches (approximately 15% higher than the circuit of Fig. 1 without the auxiliary circuit). This causes about 30% higher conduction losses in both the primary switches. With the advent of low on-resistance MOSFET switches, the conduction losses of the primary switches are significantly lower than the switching losses, particularly at very high operating frequencies. After making trade-offs in selecting various circuit parameters for the wider input voltage range, the experimental results, as given in Fig. 14,

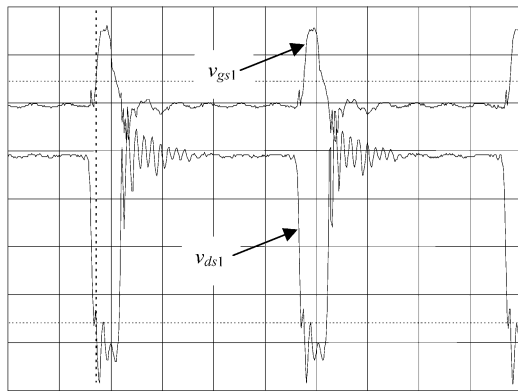


Fig. 11. Waveforms at turn-on of switch S_1 : Top trace: gate signal (5 V/div, 0.5 μ s/div), Bottom trace: drain-to-source voltage (20 V/div, 0.5 μ s/div).

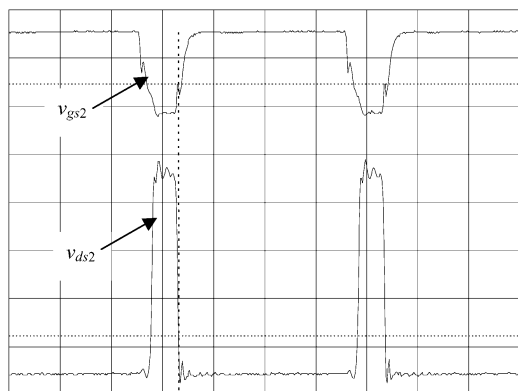


Fig. 12. Waveforms at turn-on of switch S_2 : Top trace: gate signal (5 V/div, 0.5 μ s/div), Bottom trace: drain-to-source voltage (20 V/div, 0.5 μ s/div).

show that the modified APWM resonant converter has near constant and higher efficiency as a function of input voltage than the circuit without the auxiliary network given in [7].

VI. EXPERIMENTAL RESULTS

To verify this modified topology, a 35 W converter with dual 5 V outputs was constructed. The input voltage is 80 V and the switching frequency is 500 kHz. In the resonant circuit, the following values were used: the resonant capacitor was 22 nF, the resonant inductor was 6.5 μ H and the transformer turn ratio was 2.5 to 1. The value of the auxiliary inductor used was 6 μ H, therefore K was close to 1. The capacitors in the auxiliary circuit (C_{1a}, C_{2a}) were chosen as 2.2 μ F.

The main goal of the modified topology is to achieve ZVS for higher input voltages. Figs. 11 and 12 show the effect of ZVS at the turn-on of switches S_1 and S_2 . In both figures, the dotted vertical line shows that the drain-to-source voltage reaches zero before the gate signal is applied.

VII. COMPARISON BETWEEN ORIGINAL APWM CONVERTER AND MODIFIED TOPOLOGY

The mode of operation described in Section III is similar to the operation of the original APWM resonant dc/dc converter, yet at higher voltages ZVS is lost while this new topology maintains it. Notice that for S_2 to achieve ZVS, the resonant current (which is also the current that flows through the switches) at

the turn-off of S_2 must have enough negative current in order to discharge C_1 to zero volts for ZVS to occur. This condition cannot be satisfied at higher input voltage in the original APWM converter. For example, at $V_{in} = 80$ volts, Fig. 13 shows the switching waveforms of the original circuit ([7, Fig. 1]) and the modified topology. It can be seen that ZVS is lost for S_1 in the original circuit because the resonant branch doesn't supply enough negative current to discharge C_1 . With the addition of the auxiliary branch in the modified circuit, however, it supplies the additional current to the switch to discharge C_1 and achieve ZVS. The current through this auxiliary branch acts as a compensation for the resonant current when the input voltage increases whereas earlier the original APWM was limited to a narrow range of input voltage.

Fig. 14 shows the efficiency, η , of the modified topology and the original one in relation with the input voltage using the same experimental set-up in Section VI (with the diode rectifier). It is easily seen that overall the modified topology has a higher efficiency than the original design, but this is more evident at higher voltages. The efficiency of the original design begins to fall when the input voltage is higher than 55 V. This is due to the loss of ZVS at higher input voltages as explained earlier. The efficiency of the modified topology however is consistent at 83% throughout the whole input voltage range with a variation of about 1% due to the fact that ZVS is maintained. Furthermore, the use of synchronous rectifiers in the circuit results in overall efficiency greater than 90% at 500kHz switching frequency.

It has just been described how the auxiliary inductor of the modified circuit acts as a compensation for the resonant branch. That means, in the modified circuit, smaller Q_o can be selected to maintain ZVS over a wide input voltage range, while reducing the voltage stress on the resonant component. For example, the curves of voltage, $v_{Ls}(t)$ across the resonant inductor are shown in Fig. 15 with $Q_o = 1.5$, in the original circuit and $Q_o = 2.5$ in the modified circuit. As it can be seen from Fig. 15, the inductor voltage of the original circuit is higher and will have notably higher frequency harmonics and thus higher core losses compared to the modified topology with $Q_o = 1.5$. The significant reduction in core losses of the modified topology will make the resonant inductor much easier to manufacture. However, as explained in Section V, the minimum value of Q_o should be limited to minimize the circulating current in the switch.

Like the original circuit, the modified converter can also be operated at near no-load. As the auxiliary circuit provides ZVS for both the switches independent of the load current, the converter can be operated with very small duty cycle or go into the hiccup mode to achieve the no-load operation. Unlike, the original circuit, there is no need to design the output transformer with some air gap to obtain lower value of the magnetizing inductor to achieve ZVS at no-load. This helps in simplifying the design and manufacturing of the transformer in the modified topology.

VIII. CONCLUSION

This paper has presented a modified design of the APWM resonant dc/dc converter topology. Its operating principle and steady-state analysis have been described in detail. It has been

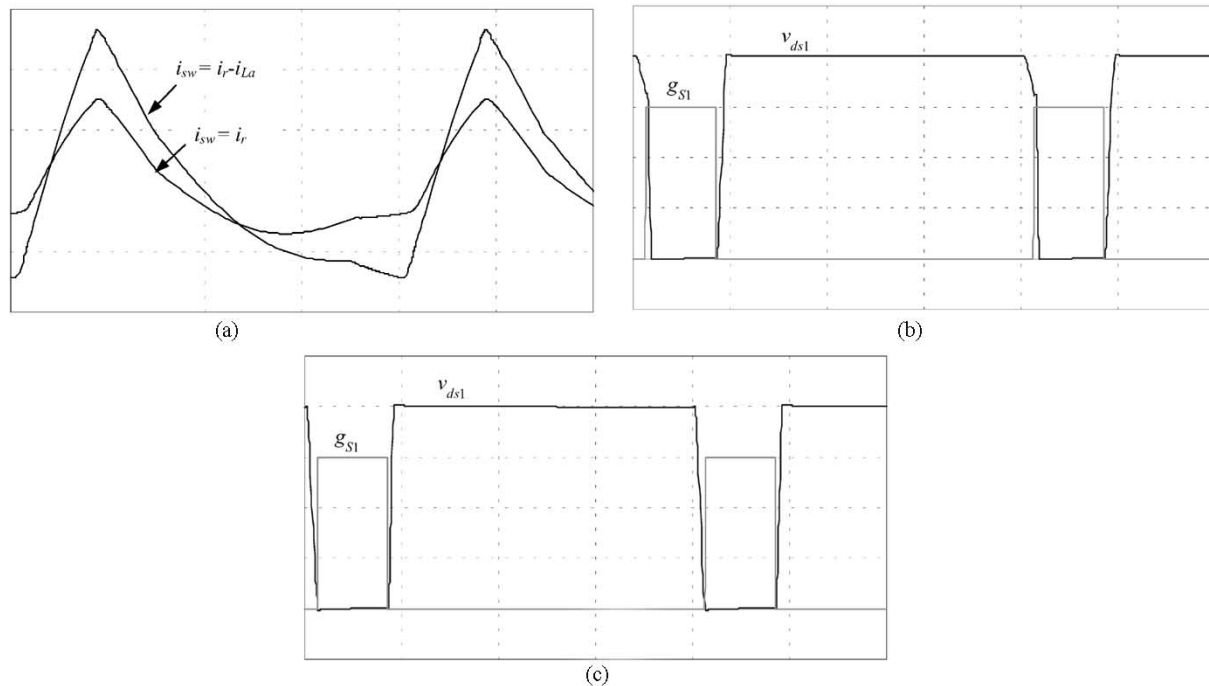


Fig. 13. Switching waveforms of original and modified APWM resonant dc/dc converter with $K = 1$, $Q_o = 1.5$ and $\omega = 1.1$ (Time scale: $0.5 \mu\text{s}/\text{div}$). (a) Switching current i_{sw} (2 A/div): $i_{sw} = i_r$ in original circuit, and $i_{sw} = i_r - i_{La}$ in modified circuit. (b) Original circuit: Gating signal and drain-source voltage (20 V/div) of S_1 . (c) Modified circuit: Gating signal and drain-source voltage (20 V/div) of S_1 .

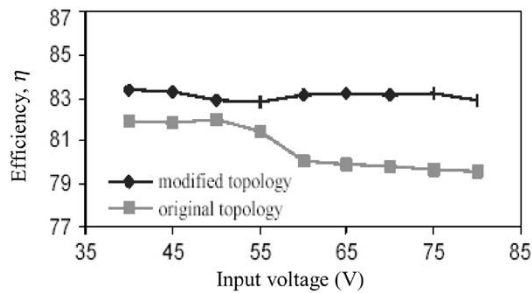


Fig. 14. Efficiency of original APWM resonant converter and modified topology with variation of input voltage (switching frequency = 500 kHz, resonant frequency = 454 kHz).

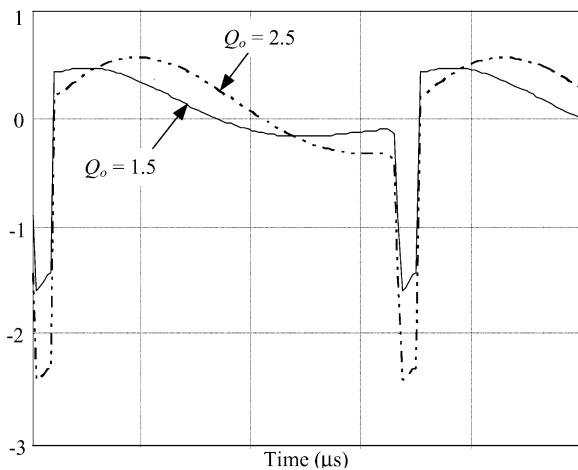


Fig. 15. Voltage across resonant inductor for $Q_o = 2.5$ (original circuit) and $Q_o = 1.5$ (modified circuit).

proved with the aid of performance curves and experimental results that the modified topology achieves ZVS over a wider input

voltage range than the original design. The converter also maintains near constant efficiency from low-to-high input voltage. The use of synchronous rectifiers in the circuit results in overall efficiency greater than 90% at 500 kHz switching frequency.

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